

REMARKS

Claims 2-8 are all the claims pending in the application. Claims 2-7 are allowed. The Examiner has withdrawn the allowability of claim 8 and has rejected claim 8 under 35 U.S.C. § 102(e) as being anticipated by Kejriwal et al. (U.S. Patent No. 6,704,794; hereinafter “Kejriwal”). Applicant submits the following in traversal of the claim rejections.

Applicant respectfully submits that claim 8 is patentable because each and every element of the claim is not disclosed or suggested by Kejriwal. Claim 1 recites:

A multi-layered packet processing device, comprising:
an interface of a public network for transmitting a data packet to a node and receiving the data packet from the node through a public network; and
a plurality of packet processing portions for sequentially processing the data packet in a pipeline pattern, according to a header of the data packet transferred from the interface of the public network, wherein each of the plurality of packet processing portions receives the data packet.

As previously noted in the Amendment of March 14, 2005, Kejriwal fails to disclose or suggest a plurality of packet processing portions for sequentially processing the data packet in a pipeline pattern, according to a header of the data packet transferred from the interface of the public network. Although the Examiner states that the packet processing pipeline 240 and the output packet organizer 250 correspond to the aforementioned features of claim 1, none of these components processes the data packet.

The specification of Kejriwal is clear in disclosing that the packet processing pipeline 240 and the output packet organizer 250 do not process the data packet itself, but merely handles control information:

The type of information processed by packet processing pipeline 240 and entered into output packet organizer 250 is typically control information not random customer data. For example, *information located within the various headers associated with a packet (along with other control information as discussed below) is directed to packet processing pipeline 240 from packet aggregation layer 205. Packet aggregation layer 205 is therefore typically designed to extract or copy a packet's header information for presentation to the packet processing pipeline 240.* Col. 4, lines 18-27.

Specifically, the packet processing pipeline 240 receives *control information* through the packet processing pipeline input 270a. The output packet organizer 250 then receives a *packet identifier* from the packet processing pipeline 240. Col. 4, lines 37-40. As shown by the cited passage above and Fig. 1B, the packet 152 is not transmitted to the packet processing pipeline 240 nor the output packet organizer 250. Instead of transmitting the data payload of the packet 152, only the header information is transmitted to the packet processing pipeline 240.

Therefore, Kejriwal cannot possibly disclose the plurality of packet processing portions as claimed.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

RESPONSE UNDER 37 C.F.R. § 1.116
U.S. APPLN NO.: 09/899,531

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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